Technical Notes on using Analog Devices' DSP components and development tools
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Considerations for FLASH PROMS with Timing Requirements

By H.D.

Question:

I need to know the minimum time between the rising edge of /RESET and the falling edge of /BMS when EBOOT is high and LBOOT is low. This parameter is important since flash PROMS also have a /RESET input and a minimum timing requirement between the rising edge of /RESET and falling edge of /CS and /OE. I may need to implement an early /RESET for the flash PROM, but until I know how soon the SHARC asserts /BMS, I don't know how much earlier the PROM needs to be reset.

Answer:

The following applies only to the 21060/60L, 21062/62L and 21061/61L:

If the first cycle that RESET is deasserted (goes high) is cycle #1, then BMS will be asserted (go LOW) in cycle #6.

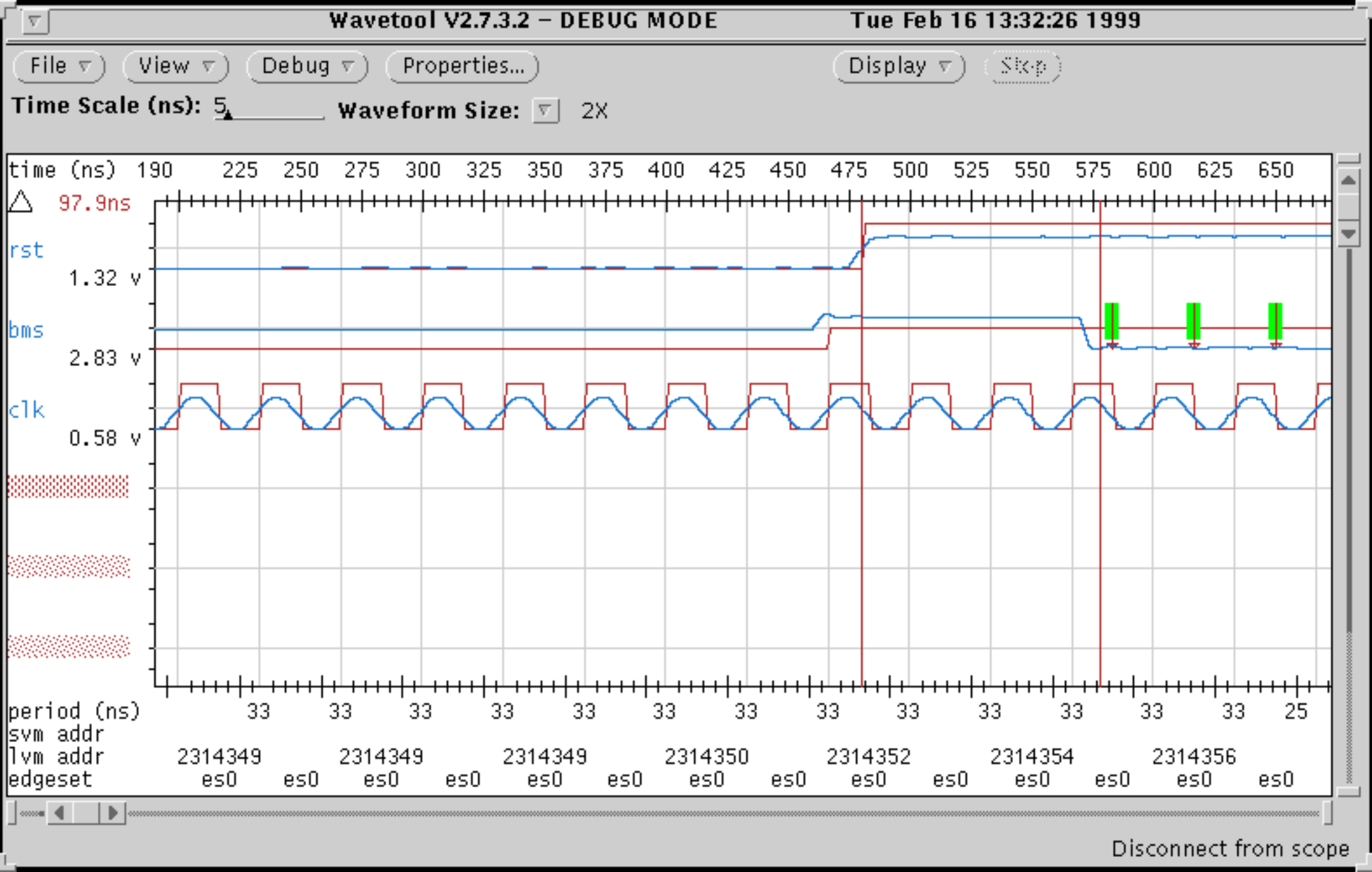
The following applies only to the 21065L:

If the first cycle that RESET is deasserted (goes high) is cycle #1, then BMS will be asserted (go LOW) in cycle #4.

Note: A cycle is defined as a CLKIN cycle. ie: if CLKIN is 30MHz, a cycle is 33.3ns in length.

Attached is a waveform for the 21065L from a digital scope that should help make this clear.

ANALOG DEVICES


Wavetool V2.7.3.2 – DEBUG MODE
Tue Feb 16 13:32:26 1999
File
View
Debug
Properties...
Display
Skip
Time Scale (ns): 5
Waveform Size: 2X
time (ns) 190 225 250 275 300 325 350 375 400 425 450 475 500 525 550 575 600 625 650
97.9ns
rst
1.32 v
bms
2.83 v
clk
0.58 v
period (ns) 33 33 33 33 33 33 33 33 33 33 33 33 33 33 25
svm addr
lvm addr 2314349 2314349 2314349 2314350 2314352 2314354 2314356
edgeset es0 es0 es0 es0 es0 es0 es0 es0 es0 es0 es0 es0 es0 es0
Disconnect from scope